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IVO Product Information

Product Name: M236MWF2 R0

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2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by IVO for any intellectual property claims or other problems that may result from application based on the module described herein.

FQ-7-30-0-009-03D

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1 Introduction

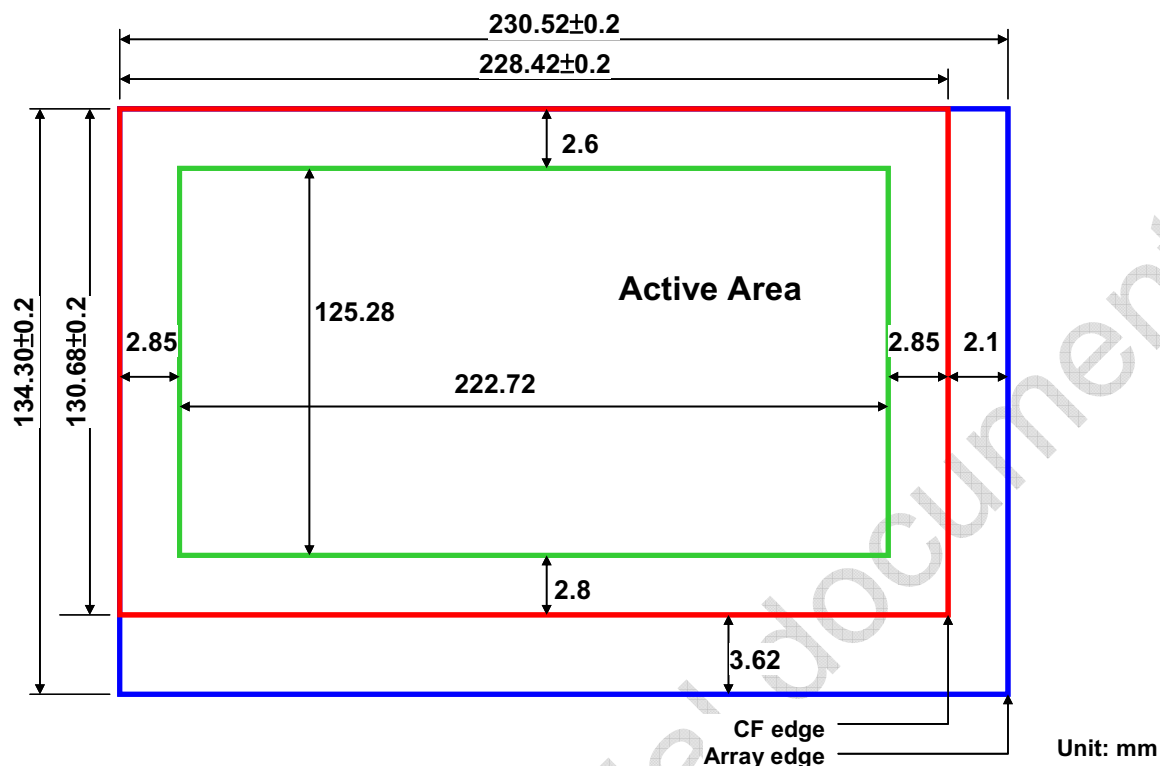
C101NWTG-1 is a Color Active Matrix Liquid Crystal Display composed of 4 Chip TN TFT LCD Cell. The format of screen is intended to support the WXGA(1024 (H) x 600(V)).

2 General Characteristics

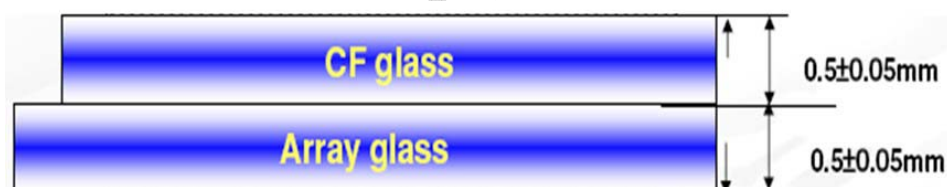
Item		Specification	Unit	Remark
Active Area (W x H)		222.72(H) x 125.28(V)	mm	Single chip
Number of Dots (H x V)		1,024 (x3) x 600	dot	Single chip
Pixel Size (W x H)		0.2175(H)x0.2088(V)	mm	Single chip
Dimension (W x H x t)		245.72x 544.32x1.00	mm	Not include separator
Display Mode		Normally White (TN)		
View Direction		6 o'clock		
Temperature Range	Storage	-20 to 60	℃	
	Operating	0 to 50	℃	
Response Time		8(Typ.)	ms	With IVO requirement driving condition, Refer to 10
Contrast Ratio		(500)		
Viewing Angle	L/R/U/D	70/70/50/70 (Typ.)	deg.	CR ≥ 10 with IVO requirement driving condition, Refer to 10
Chromaticity	NTSC Ratio	45% (Typ.)	%	With reference back light spectrum, see in 11 (Cell with reference polarizer)
	White	0.313±0.03 0.329±0.03		
	R	TBD		
	G	TBD		
	B	TBD		
Panel Transmittance		(6.36)	%	
Color Filter Structure		Stripe RGB		
Weight	4 Chip (1/10cut)	(416.51)	g	without POL

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3 Outline size of Cell (single chip)



4 Cell Thickness (single chip)

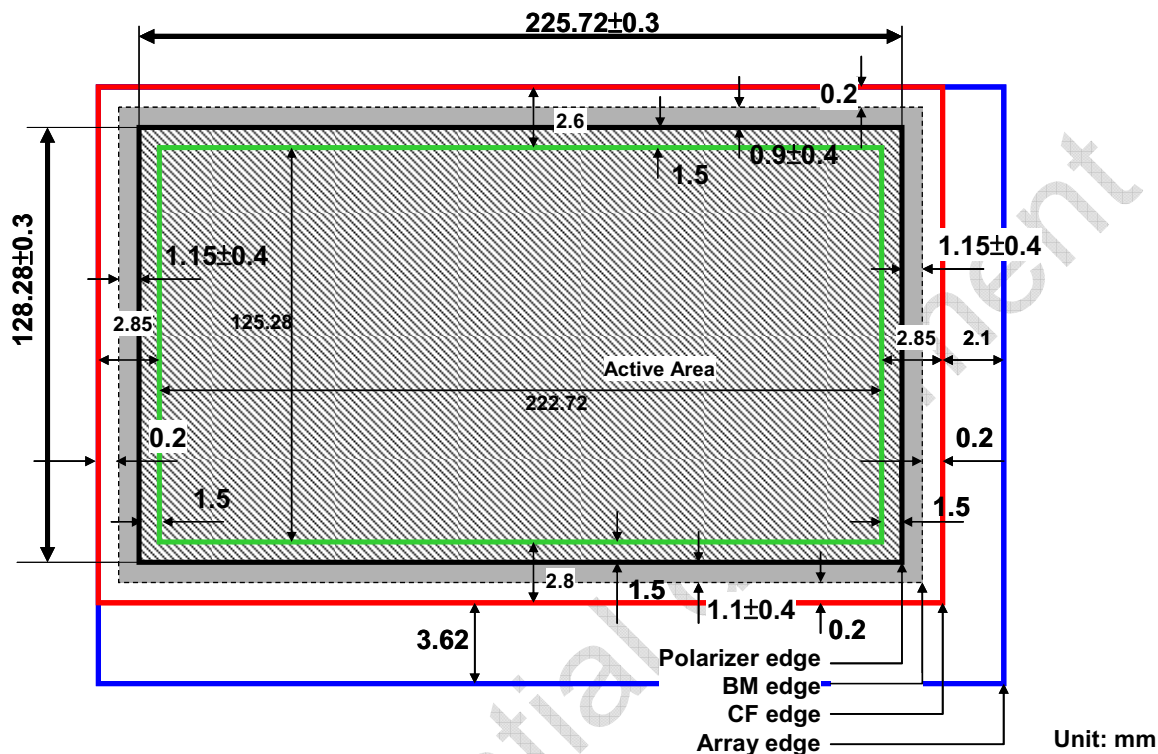


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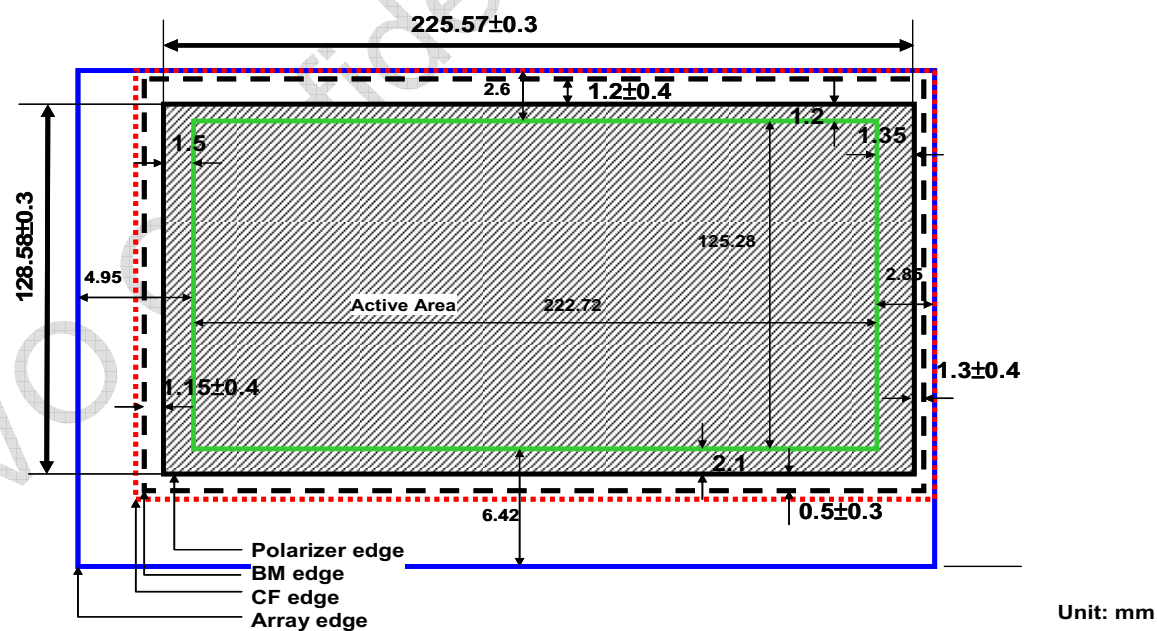
5 Polarizer Attachment Direction and Size (single chip)

5.1 Polarizer Attachment Direction

Polarizer on CF side



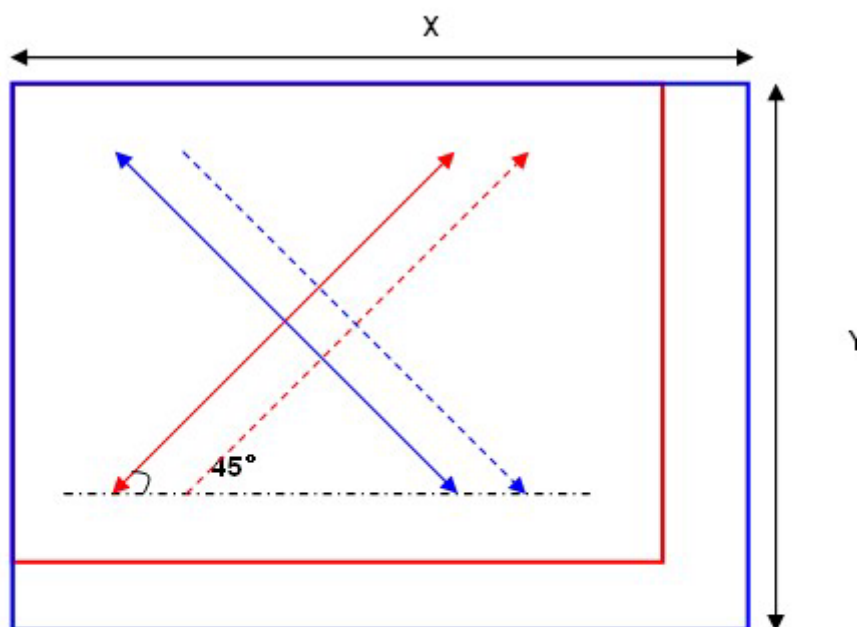
Polarizer on array side



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5.2 View from Array film side

View from Array film side



CF side polarizer absorption axis



TFT side polarizer absorption axis



CF side rubbing direction



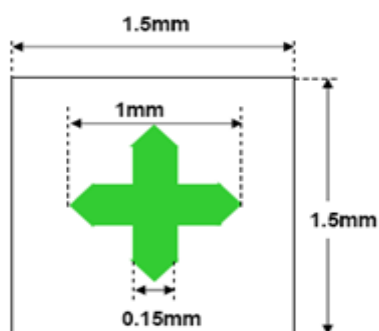
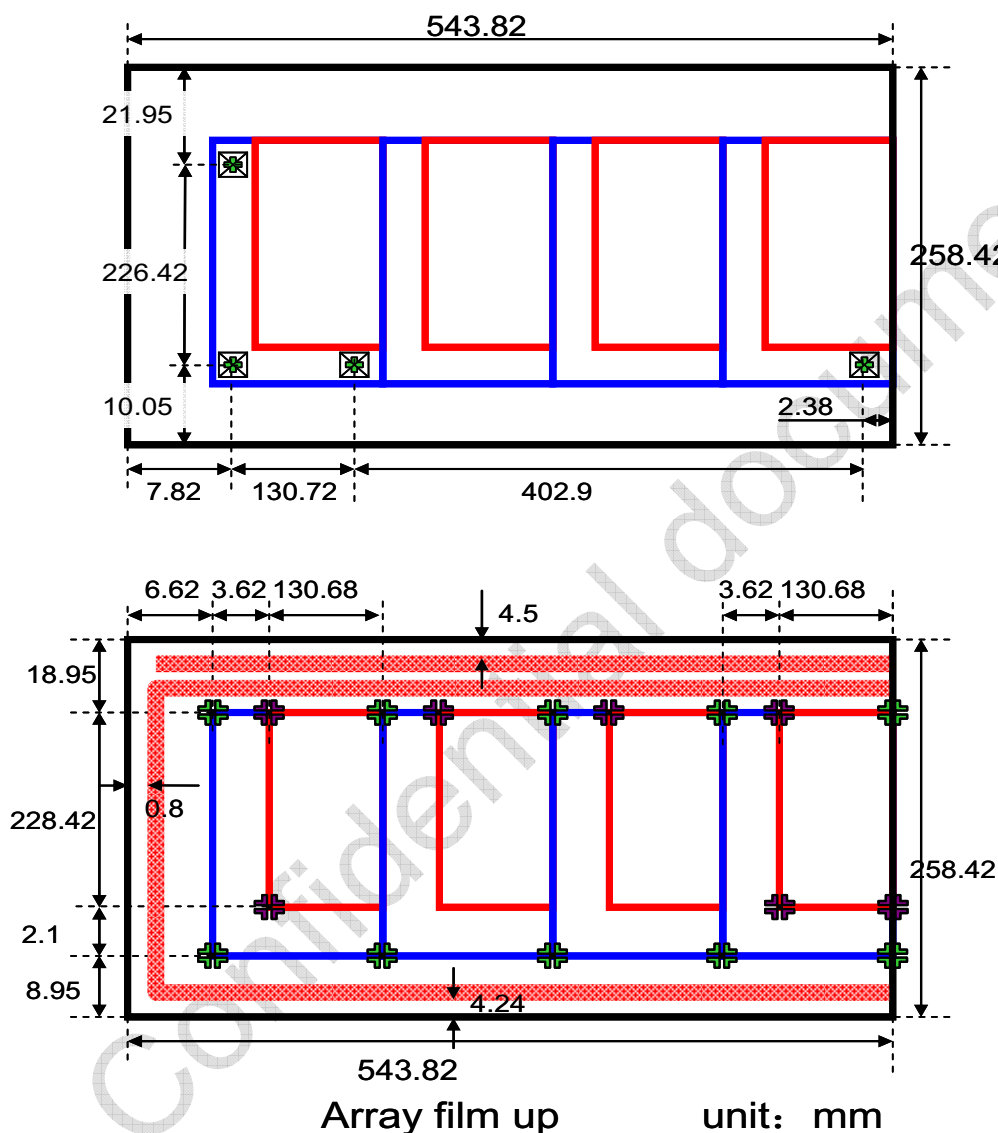
TFT side rubbing direction

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6 1/10 substrate's size and cutting alignment mark

6.1 1/10 Substrate's Size

Sub A: 543.82x258.42



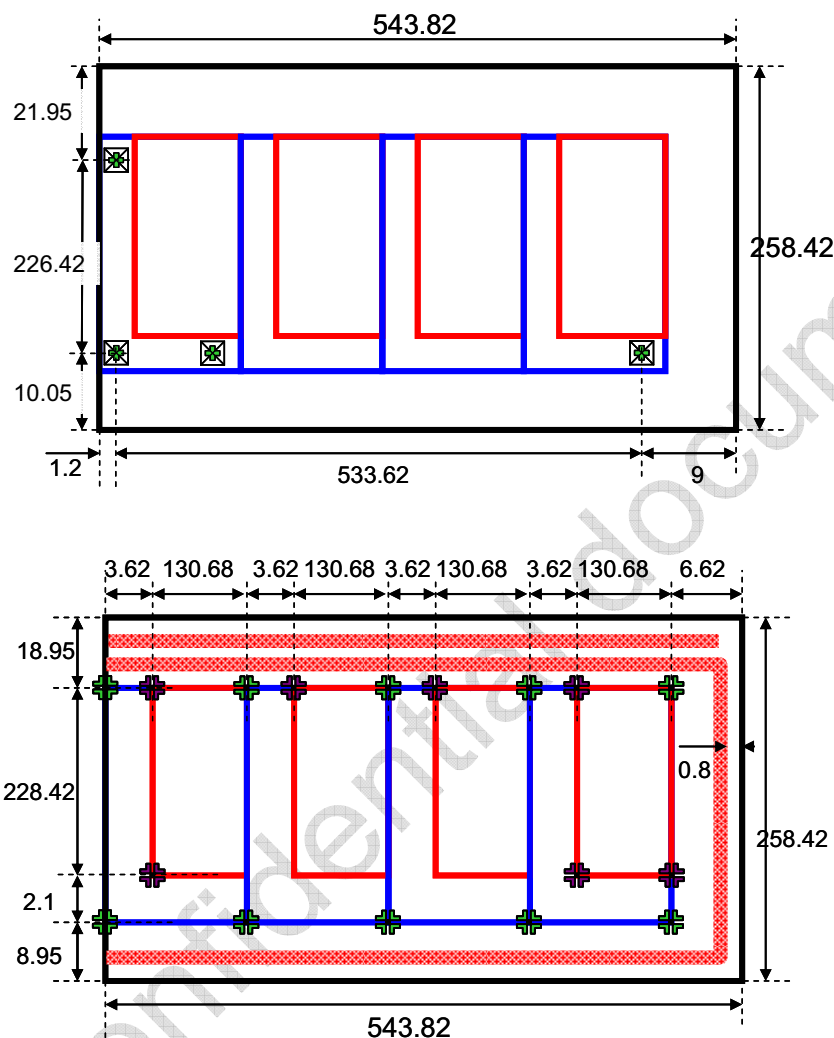
Cutting alignment Mark



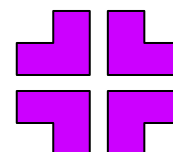
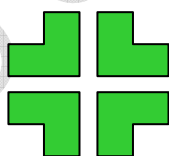
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6.2 Cutting Accuracy Mark

Sub B: 543.82x258.42



Array film up unit: mm



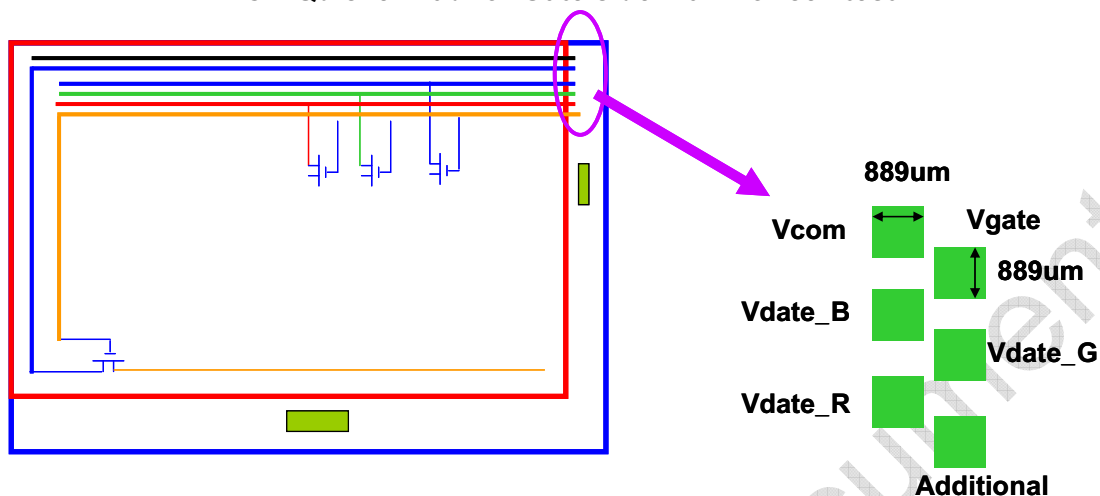
Cutting accuracy mark on TFT

Cutting accuracy mark on CF

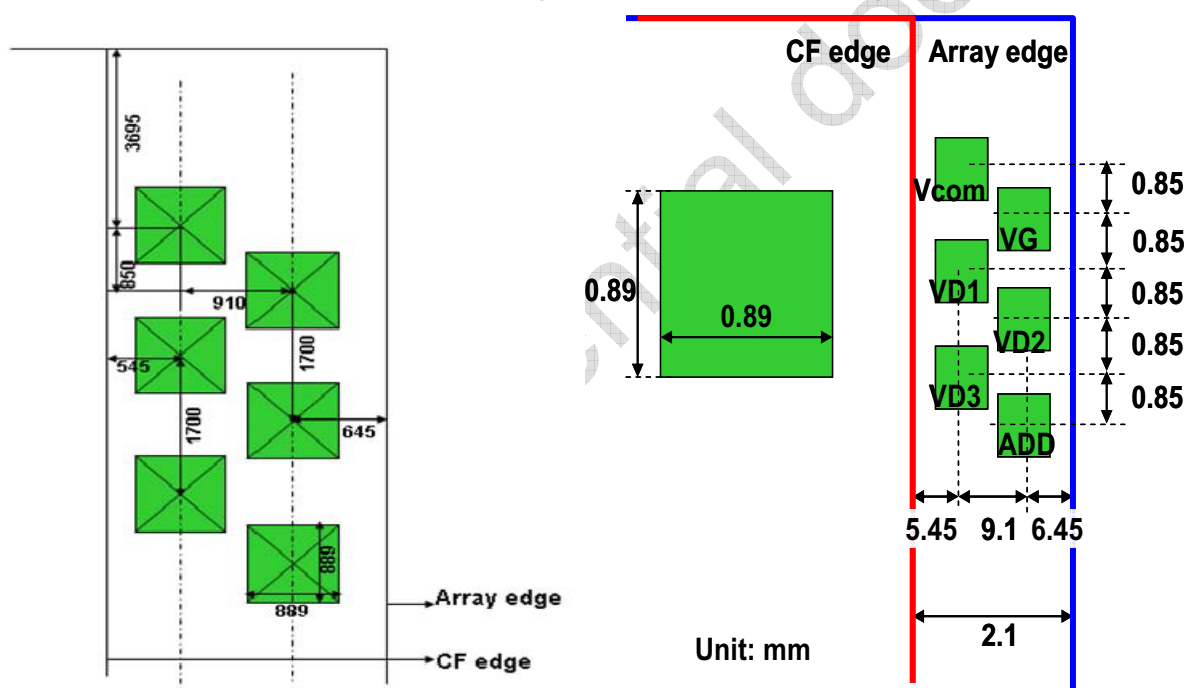
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6.3 Cell Light-On Test Pad Drawing (Shorting bar)

LCD Quicker Pad for Gate side mark for cell test

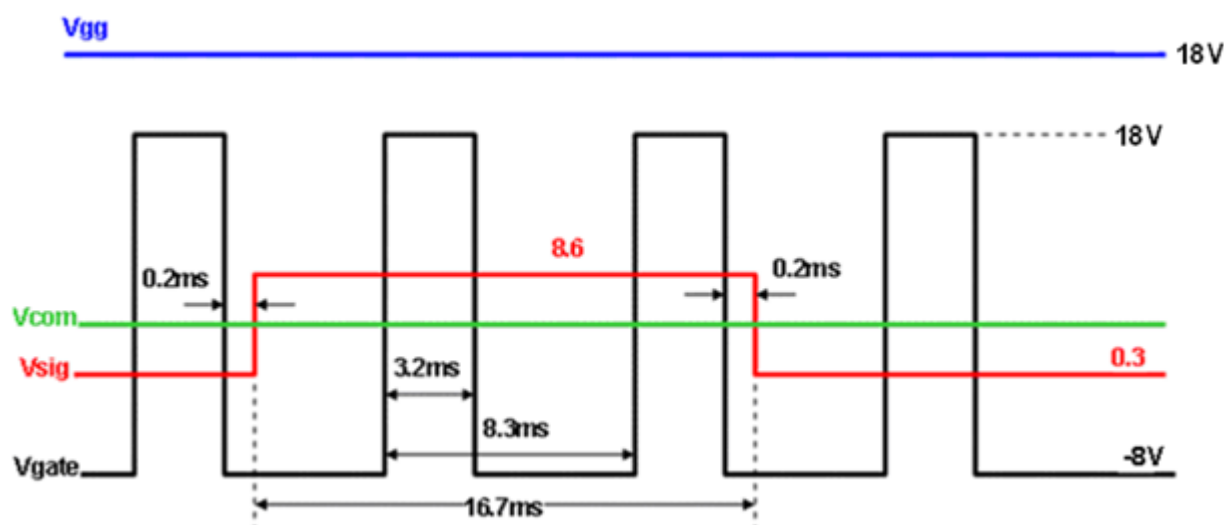


Cell testing pad dimension drawing



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6.4 Cell Light-On Test Waveform(Shorting bar)



Pattern:

Black: VData_1, VData_2 and VData_3 input same as Vsig: 8.6V/0.3V; Vcom is DC3.7V.

Gray: VData_1, VData_2 and VData_3 input same as Vsig: 6V/2V; Vcom is DC3.55V.

White: VData_1, VData_2 and VData_3 input same as Vsig: 3.55V; Vcom is DC3.55V.

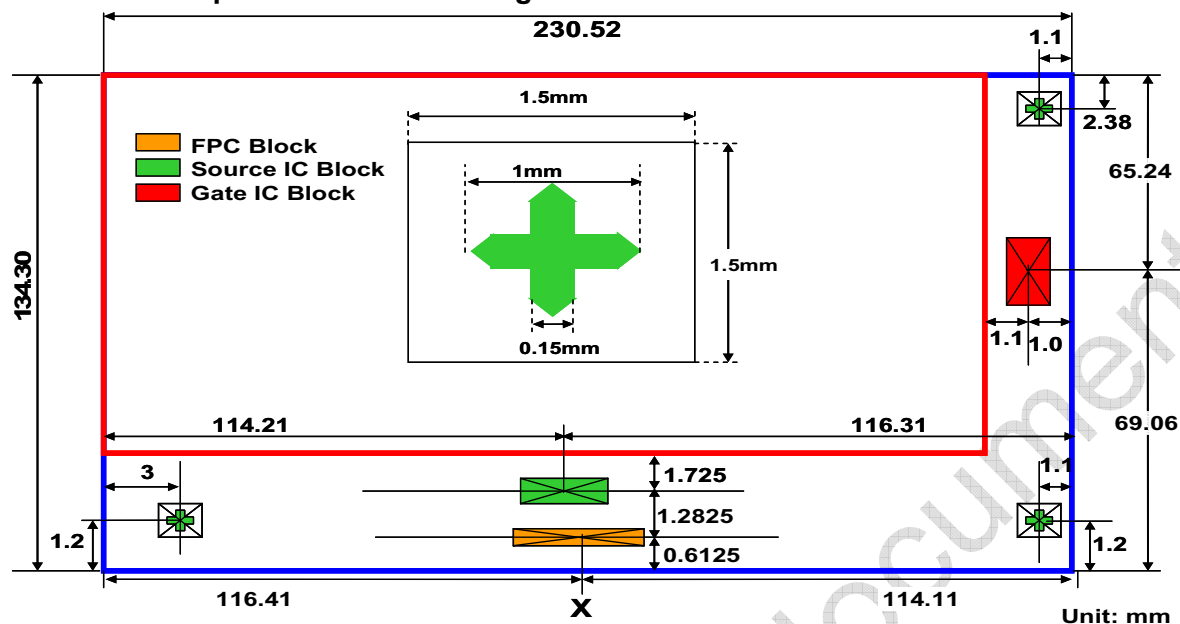
Yellow: VData_1 input same as Vcom 3.7V; VData_2 and VData_3 input same as Vsig: 8.6V/0.3V; Vcom is DC3.7V.

Fuch sine: VData_2 input same as Vcom 3.7V; VData_1 and VData_3 input same as Vsig: 8.6V/0.3V; Vcom is DC3.7V.

Cyan: VData_3 input same as Vcom 3.7V; VData_1 and VData_2 input same as Vsig: 8.6V/0.3V; Vcom is DC3.7V.

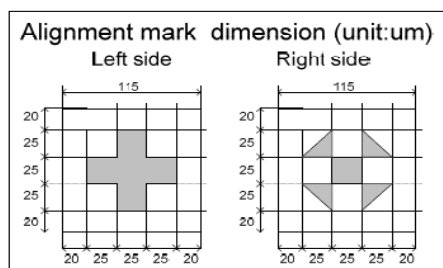
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7 Gate COG Chip/Source FPC Bonding Pad Location



7 COG Dimension

7.1 X_COG



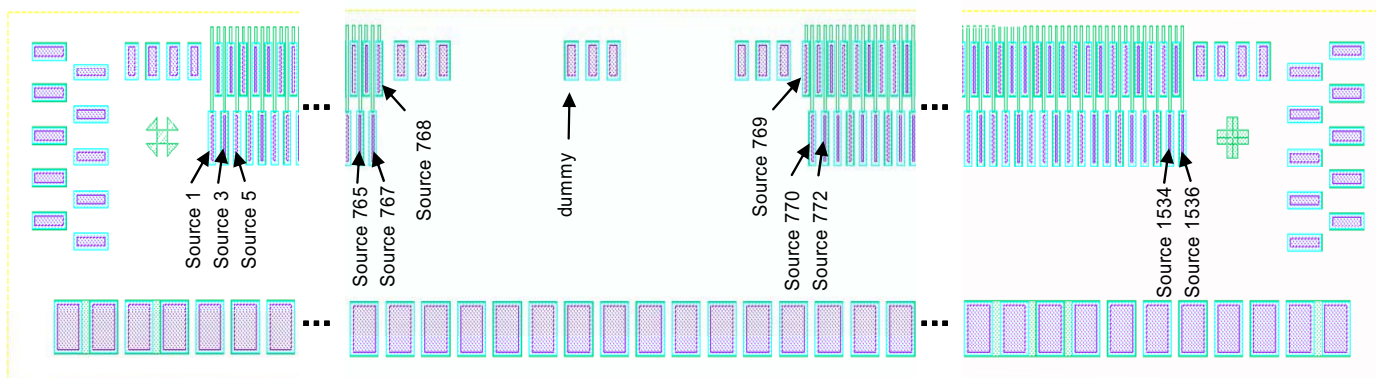
Symbol	Dimension (um)
A	15
A1	30
A2	100
A3	30
B	30
B1	50
B2	70
B3	50
B4	50
C	65
C1	85
C2	100

Symbol	Dimension (um)
D	30
D1	40
D2	80
D3	43
D4	33
D5	96
D6	74
D7	20
E1	25000
E2	700
E3	256
E4	57(max)
E5	57(max)

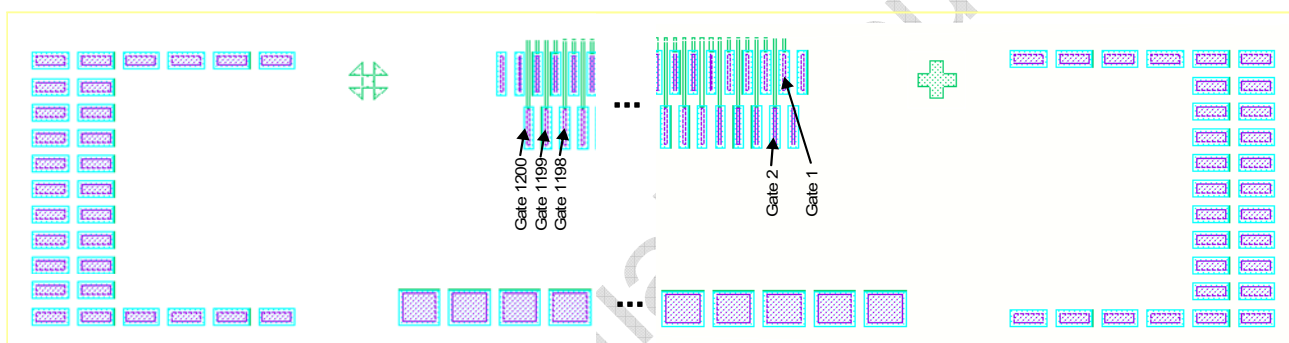
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8 Cell Electrode Pin Assignment

8.1 From Source Data Side Pin Assignment



8.2 From Gate Side Pin Assignment.



Array edge



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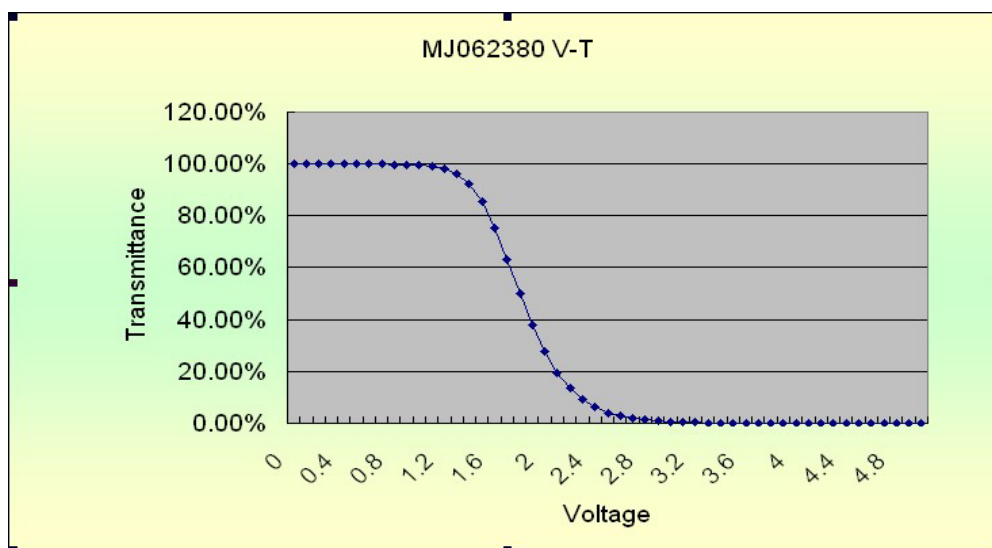
8.3 FPC Pin-assignment X- /Y- Driver

No.	pin	No.	pin	No.	pin	No.	pin	No.	pin
1	VCOM	34	IFSEL	67	G1	100	V5	133	VDD
2	VCOM	35	MODE	68	G2	101	V4	134	VDD
3	VCOM	36	OPDRV	69	G3	102	V3	135	GND
4	NC	37	CABC EN[1]	70	G4	103	V2	136	GND
5	NC	38	CABC EN[0]	71	G5	104	V1	137	GND
6	REPO	39	VDD	72	G6	105	AGND	138	GND
7	REPI 2	40	VDD	73	G7	106	AGND	139	AVDD
8	S1	41	GND	74	DASHD	107	AGND	140	AVDD
9	VDDN	42	GND	75	VDD LVDS	108	AGND	141	AVDD
10	VDDN	43	AVDD	76	VDD LVDS	109	AVDD	142	AVDD
11	NC	44	AVDD	77	DASHD	110	AVDD	143	AGND
12	NC	45	AVDD	78	NINC	111	AVDD	144	AGND
13	NC	46	AGND	79	PINC	112	AVDD	145	AGND
14	NC	47	AGND	80	DASHD	113	GND	146	AGND
15	NC	48	AGND	81	NIND0	114	GND	147	S1536
16	AGND	49	V14	82	PIND0	115	GND	148	REPI 1
17	AGND	50	V13	83	DASHD	116	GND	149	VCOM
18	AGND	51	V12	84	NIND1	117	VDD	150	VCOM
19	AGND	52	V11	85	PIND1	118	VDD	151	VCOM
20	AVDD	53	V10	86	DASHD	119	VDD	152	XON
21	AVDD	54	V9	87	NIND2	120	VDD	153	XON
22	AVDD	55	V8	88	PIND2	121	SCL	154	VGH
23	AVDD	56	DASHD	89	DASHD	122	SDA	155	VGH
24	GND	57	R0	90	NIND3	123	CSB	156	VEE
25	GND	58	R1	91	PIND3	124	SEL1	157	VEE
26	VDD	59	R2	92	GND LVDS	125	SEL0	158	VEE
27	VDD	60	R3	93	GND LVDS	126	FRAME	159	NC
28	UPDN	61	R4	94	GND LVDS	127	DITHER	160	VCC
29	SHLR	62	R5	95	DEN	128	DIMO	161	VCC
30	GRB	63	R6	96	HSD	129	PINCTL	162	NC
31	STBYB	64	R7	97	VSD	130	DIMI	163	GND
32	DCLKPOL	65	DASHD	98	V7	131	VDD	164	GND
33	BIST	66	G0	99	V6	132	VDD	165	GND

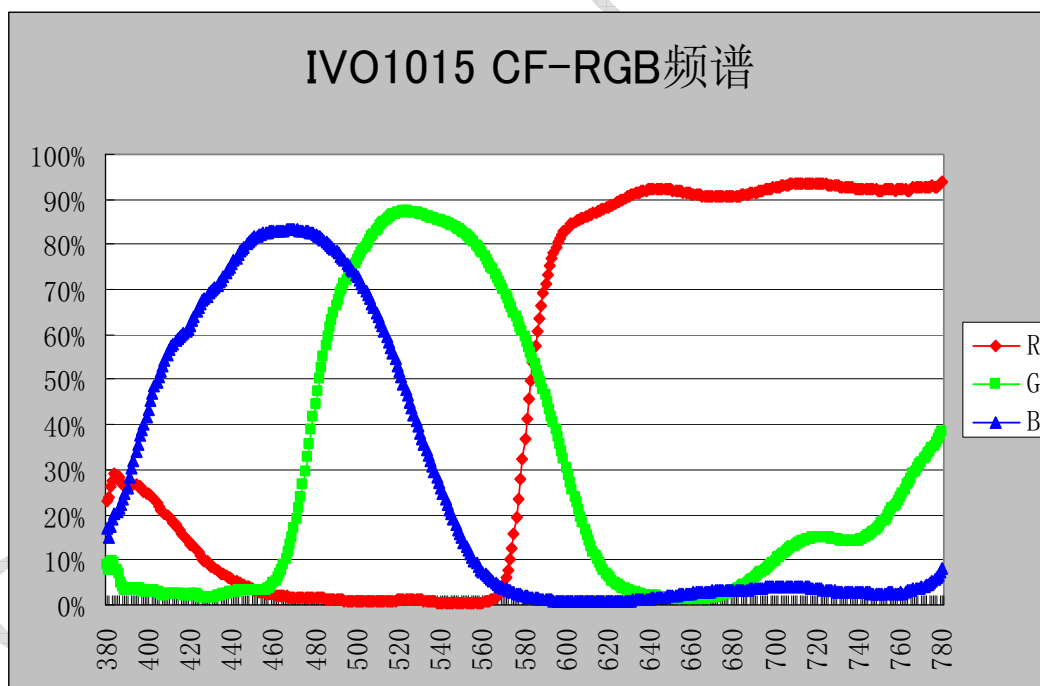
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9 V-T Curve

9.1 V-T Curve



9.2 CF Spectrum



※ Measured at ambient temperature 25℃, under IVO requirement Driving Condition (refer to see 10)

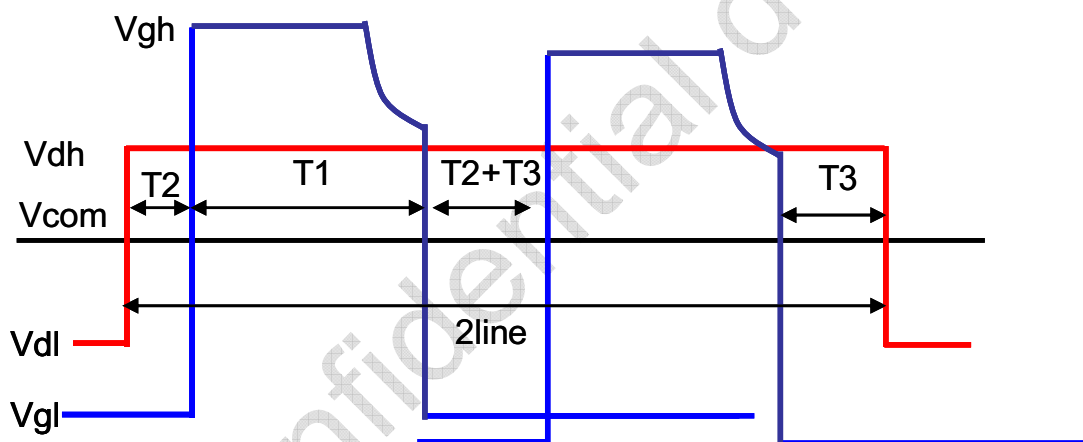
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10 IVO Requirement Driving Condition

10.1 Timing Range

Category	Parameter	Unit	min	typ	max
Timings	Frame rate	Hz	55	60	65
Scanning Method	Gate scanning method (single / double)	single			
	Inversion method	2V1H			
Line Impedance	Capacitive load of a signal line	pF	55.36	81.32	107.58
	Capacitive load of a gate line	pF	121.16	216.08	242.32
	Resistance load of signal line	KOhm	3.25	4.15	7.85
	Resistance load of gate line	KOhm	1.64	1.92	2.31

10.2 2V1H



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No.	Item	MIN	TYP	MAX
1	Vcom voltage	2.2V	3.2V	4.2V
2	Vgl voltage	-9V	-8V	-7V
3	Vgh voltage	18V	19V	20V
4	Vdl voltage	0	0.2V	0.7V
5	Vdh voltage	7.2V	8.2V	9.2V
6	Gate line charging time(T1)		11us	
7	Data line pre-opening time(T2)		0	
8	Data line delay closing time(T3)		2.3us	
9	2Line=2*(T1+T2+T3)		26.6us	
10	Dummy gate line signal	Vgl	Vgl	Vgl

10.3 OLB Outline

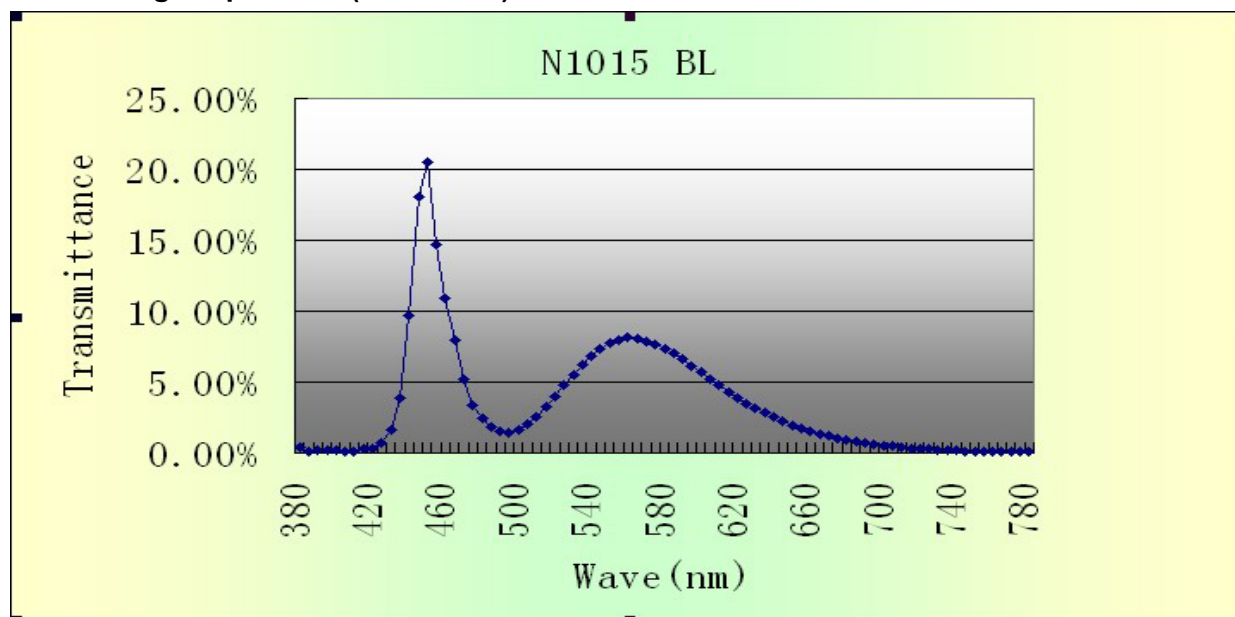
	Source Driver	Gate Driver
Output Channels	1536	1200
Driver Amount	1	1
Component Type	COG	COG
OLB Side Lead Pitch	-	-

10.4 Driver Recommendation

	Source Driver	Gate Driver
Driver Supplier and Model No	Novatek-NT51008	Novatek-NT52003

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11 Back light Spectrum (Reference)



12 IVO Recommended Cell Packaging TBD

13 Terms Definition

OLB : Outer Lead Bonding

Transmittance: Cell transmittance at all white Driving Condition.